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Raptor Codes Performance Analysis on WI MAX Technology with high speed FFT/IFFT

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Abstract

There are currently a large variety of wireless access networks, including the emerging vehicular ad hoc networks (VANETs). A large variety of applications utilizing these networks will demand features such as real-time, high-availability, and even instantaneous high-bandwidth in some cases. Therefore, it is imperative for network service providers to make the best possible use of the combined resources of available heterogeneous networks (wireless area networks (WLANs), Universal Mobile Telecommunications Systems, VANETs, Worldwide Interoperability for Microwave Access (WI-MAX), etc.) for connection support. When connections need to migrate between heterogeneous networks for performance and high-availability reasons, seamless vertical handoff (VHO) is a necessary first step. In the near future, vehicular and other mobile applications will be expected to have seamless VHO between heterogeneous access networks. Time-hopping ultra wideband (TH-UWB) and direct-sequence ultra wideband (DS-UWB) systems are among the standards proposed for UWB communications scenarios. A general unified mathematical approach has been proposed for calculating the bit error rate (BER) for both TH-UWB and DS-UWB systems in the presence of multiple-user interference and strong narrow-band interference in a multi-path scenario. Unlike many other mathematical models that provide upper or lower bounds for BER, this model calculates the exact values for BER in given scenarios. A partial rake receiver has been chosen as the receiving terminal. The modified Salem-Valenzuela channel model has been used in this analysis. The model can assess the effect of any given narrow-band interfering systems.

Keywords: *High availability, intersystem handover, load balancing, mobility management, quality-of-service (QOS), Antennas synthesis, Galileo/WI-Max bands, multiband antennas*

I. INTRODUCTION

Ultra wideband (UWB) emergence holds great promise for low cost, high data rate indoor telecommunications. This technology aims to dominate the indoor applications by facilitating wireless communication with rates as high as 110 MB/s over short ranges. According to the Federal Communications Commission (FCC) definition, any radio transmission whose bandwidth goes beyond 20% of its carrier frequency or has instantaneous bandwidth in excess of 500 MHz is considered to be UWB. Signals with such specifications, have been restricted to operate in the 3.1–10.6 GHz frequency band, which is for unlicensed use only. Due to the fact that UWB systems make unlicensed use of their spectrum further restrictions have been made on their allowed power levels. According to FCC's ruling they can only transmit at 241.5 DBM/MHz. To provide UWB with multiple accesses, it can be combined with spread spectrum techniques such as time hopping (TH) and direct sequence (DS). These two along with other approaches such as classic impulse radio (IR) and multi band orthogonal frequency division multiplexing systems are among the standards that have been proposed for UWB systems. Used for configuring wireless MAN (Metropolitan Area Network), which uses OFDMA (Orthogonal Frequency Division Multiplexing Access).FFT/IFFT is one of the important blocks used in the OFDMA systems. By adjusting length of FFT from 128 to 2048, it can be used for different applications. We have targeted our design for Mobile WI-MAX, so preference is given 2048 point FFT/IFFT. FFT architectures are mainly classified in two ways: Memory based architecture and pipelined architecture. Popular pipelined architectures are based on radix-2 or radix-4 algorithms. Radix-4 has less computational complexity compared to radix-2 architecture. Even higher radix algorithm can also be used for the implementation to decrease the computational complexity in the design. Higher the radix, lower the computational complexity. Tradeoff for the selection of architecture is the requirement of length of FFT for the particular application.

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Raptor codes

The large file to be transmitted is partitioned into one or several so-called source blocks which are further split into k so-called source symbols, each of length T except for the last one, which can be smaller. For each source block, additional repair symbols can be generated by applying an FEC, e.g. a Raptor code. Each encoding symbol, source and repair symbols, gets assigned a unique encoding symbol identity (ESI) which identifies the symbol. Then each symbol individually or a concatenation of G consecutive encoding symbols is transmitted. Raptor is a fountain code, that is, as many encoding symbols as desired can be generated by the encoder on the fly from the source symbols of a source block of
data. The decoder is able to recover the source block from any set of encoding symbols only slightly more in number than the number of source symbols. Hence, it operates very closely to an ideal erasure code which would require only exactly the number of source symbols for recovery. The code as specified for MBMS is a systematic fountain code producing n encoding symbols **E**. The code can be viewed as the concatenation of several codes. The most-inner code is a non-systematic LT code with L input symbols **F**, which provides the fountain property
of the Raptor code. The non-systematic Raptor code is constructed by not encoding source symbols with the LT code, but intermediate symbols generated by some outer high-rate block code, that is **F** itself are code symbols generated by some code with k input symbols **D**. Finally, a systematic realization of the code is obtained by applying some pre-processing to the k source symbols **C** such that the input symbols **D** to the non-systematic Raptor code are obtained.

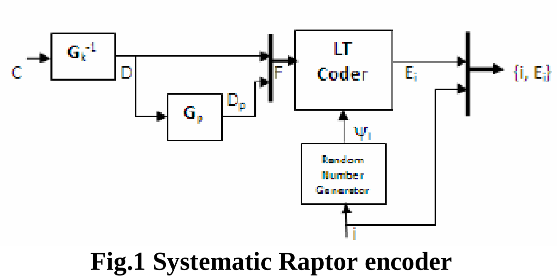

Fig.1 Systematic Raptor encoder

LT codes

LT codes are the first practical implementation of fountain codes. For each ESI i, the encoding symbol Ei is computed by randomly performing modulo-2 addition of source symbols **F**. This is done by using a random number generator that produces γi random variables uniformly distributed over [0, L−1]. The set of such numbers is denoted as Ψi. The encoding symbol degree γi itself is a random number with a given probability density function. For the standard LT
Code, the robust Soliton distribution is used. With **F** representing the symbols entering the LT encoder, and **E** the encoding symbols being produced by the LT encoder, the encoding symbols Ei for i = 1, . . . , n are generated as

$$E_i = \sum_{j=1}^{\gamma_i} F_{\psi_i}(j)$$

Note that the decoder has to be aware not only of encoding symbol Ei, but also of the ψi to make use of the received encoding symbol. This can be accomplished by either transmitting this information explicitly, or more elegantly, by applying the same random generator at both side and using the ESI i as the seed of the random generator. Let us define r**i** as a row vector with γi ones at positions ψi.

$$E_i = \Gamma_i . F$$

Furthermore, we define the generator matrix of the LT code taking into account the consecutive ESI i = 1,2, . . . , n as:

$$G_{LT}(1,2,\ldots n) = [\Gamma_1^T \Gamma_2^T \ldots \Gamma_n^T]$$

Why Channel Estimation

There is various reasons to estimate the channel. In which some are as below:-
It allow the receiver calculate the impulse response. It is used to observe the behavior of the channel. Diversity techniques (for e.g. the IS-95 Rake receiver) utilize the channel estimate to implement a matched filter such that the receiver is optimally matched to the received signal instead of the transmitted one. One of the most important benefits of channel estimation is that it allows the implementation of coherent demodulation.

II. PROPOSED ARCHITECTURE

A. Single Delay Path Feedback (SDF)

Basic module of SDF is shown in fig. 2(a). Where first N/2 input samples are stored in FIFO and operation starts when N/2+1st data is available at the input to the butterfly unit. For designing N-stage pipelined FFT/IFFT architecture same SDF module is repeated for log2N time. It gives flexibility in design of any point FFT/IFFT. SFG shown in fig. 2 can be implemented using R2SDF. Block diagram for the same is shown in figure

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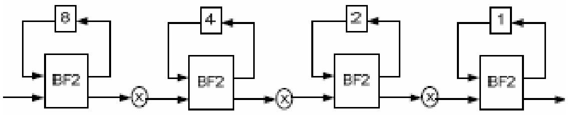

Figure 2 Pipelined architecture of 16-point FFT using R2SDF

Where 8, 4, 2 and 1 written in the FIFO field of basic module show the size of the FIFO required at different stages. Generalized pipelined stage based on SDF is given below.

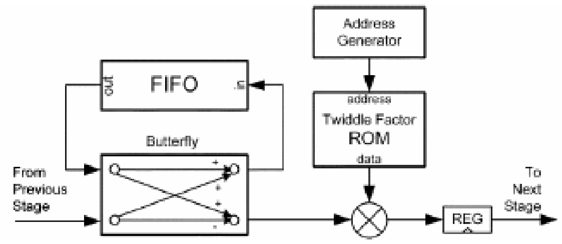

Figure 3 General pipeline stage based on SDF [5]

Modification in generalized pipeline stage is done by modifying FIFO design to enhance the throughput of the design. At different stages of the design, requirement of FIFO is different. Length of FIFO depends upon in which stage of pipeline it is used, where width of FIFO depends upon word length used. In proposed architecture we have chosen word length as 2 x 16 bits. So, width of FIFO is 32 bits. As, suggested in, we need to store first N/2 input points in FIFO. This brings the clarity to design different sized FIFO. For N-point FFT/IFFT size of FIFO for the first stage is N/2 x 32 bits, for second stage N/4 x 32 bits, so on and so forth till the end of pipeline architecture. Read and write clock of FIFO is taken on different events. This helps to improve the throughput for the pipelined architecture. Read and write operations are explained in more detail in

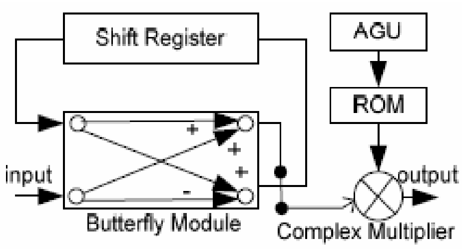

Figure 4 Proposed architecture for writing different output to FIFO

In generalized pipeline stage based on SDF, summation output of butterfly unit is stored in FIFO, and subtraction output is passed for multiplication with twiddle factor on each clock event as shown in fig. 5. In proposed architecture subtraction output is stored in FIFO and summation output is passed to the next stage without any multiplication. For the N-point FFT/IFFT first N/2 points are stored in the FIFO. N/2+1st input is directly given as the second input to butterfly module and first input comes from the FIFO as shown in fig. 5. Summation output of the butterfly is passed directly to the next stage, while subtraction output is stored back to the FIFO. When next set of input comes, subtraction outputs of butterfly unit which was stored in FIFO are passed as an input of complex multiplier to multiply necessary twiddle factor. Outputs which are first fed to the input of the next stage are propagated first in the pipeline. Idea behind this change in proposed architecture is to arrange the output as per order as required in SFG for N point radix-2 FFT/IFFT as shown in fig. 2. RTL diagram for the proposed architecture is shown in fig. 6. AGU (Address Generation Unit) which generates read address for the ROM. Through which particular twiddle factor is passed for the Multiplication.

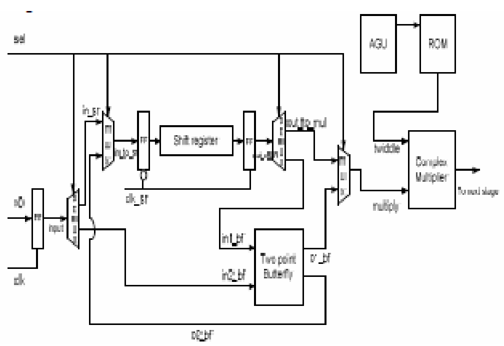

Figure 5 RTL diagram of proposed architecture

III. COMPLEXITY ANALYSIS

In this section, we will analyze the computational complexity of the proposed iterative decision feedback FDE (IDF-FDE) and frequency domain DDCE. It will show the complexity comparison of the symbol detection algorithms including the proposed IDF-FDE, iterative FDE with linear equalization (IL-FDE) and the conventional real-valued TDE. The numbers of real multiplications required per iteration to yield *N*-length time domain symbols are reported. For fair comparison, it is assumed that the conventional TDE employs *N*-tap filters with respect to *N* length block process in FDE. Note that for the first iteration of IDF-FDE, due to

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the process of overlapping data, the required real multiplications is

4Mlog2 (M) +4Nlog2 (N) +4M

From this conclusion it can be seen that the implementation of equalization in IDF-FDE scheme requires much lower complexity than TDE, and the similar complexity with IL-FDE. For the coefficients calculation, TDE still requires the highest computational complexity, while the proposed IDF-FDE needs several resources to calculate the correlation and feedback coefficients compared with IL-FDE.
For the CE algorithms, others reports the numbers of real multiplications used in the proposed DDCE, frequency domain LMS channel estimation (LMS-CE) and AFDCE. In this comparison, the *N*-length channel coefficients are estimated, and *W*-length taps Wiener filter is used in DDCE. In AFDCE, *M* denotes AR-model order. AFDCE requires the highest computational complexity, while compared with LMS-CE, DDCE employs D filter to improve the accuracy of CFR and by decreasing tap number of filters the computational complexity of DDCE can be reduced.

IV. SIMULATION RESULTS

The Raptor encoding and decoding are done according to the standard RFC 5053 proposed by the Internet Engineering Task Force (IETF). The data to be transmitted is divided among 40 source symbols, each symbol being 2 bits wide, thus constituting 640 bits. The data is encoded into 60 encoded symbols thus constituting 960 coded bits. Similarly, a rate 2/3 quasicyclic LDPC code having code length 960 is used. The expansion factor for LDPC code is 40. Fig.6 and 7 show the BER performance of Raptor codes and LDPC codes in Rayleigh fading channel for 80 and 160 burst errors respectively. Fig.4 shows the BER performance in case of end-around bursts. Fig.6 shows the BER performance for maximum of 224 burst errors, as the minimum bits needed for Raptor decoding is 736.

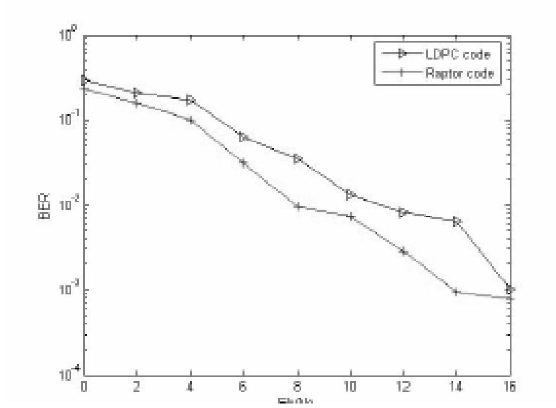

Fig.6: BER performance of Raptor and LDPC codes in Rayleigh channel with 80 burst errors

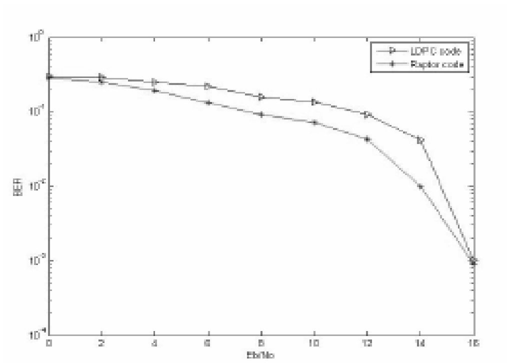

Fig.7: BER performance of Raptor and LDPC codes in Rayleigh channel with 224 burst errors

In order to investigate the performance of the proposed scheme under mobile environment, TU6 channels with 10Hz and 70Hz Doppler shift, which are realized with Jacks' model, are utilized in the simulation. It give the SER comparison versus SNR for TU6 channel with 10Hz and 70Hz Doppler shift respectively. From Fig.6 and Fig 7, it can be seen that the conventional TDE and IDF-FDE with LMS-CE cannot track time-varying Rayleigh fading channel, which result in poor performance.

V. CONCLUSION

We studied the theory of LT codes and Raptor codes and have implemented efficient encoding and decoding algorithms for Raptor codes which were proposed in the RFC 5053, "Specification Text for Systematic Raptor Encoding" .We have implemented the Raptor code and quasi-cyclic LDPC code for channel coding in OFDM. From the simulations carried out using MATLAB, the BER performance and burst error correcting capability of both the codes

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in Rayleigh fading channel are analyzed. From the simulations, we observe that the performance of Raptor codes is superior to that of Quasi-cyclic LDPC codes.

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