DIGITAL SIMULATION OF MULTI LEVEL INVERTER BASED DYNAMIC VOLTAGE RESTORER

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ABSTRACT

This paper deals with simulation of multilevel inverter based DVR. The DVR circuit produces high quality voltage since it uses a nine level inverter. This DVR gives better solution to the voltage sag problem by injecting a voltage with reduced harmonics. DVR controls the voltage applied to the load by injecting voltage of proper amplitude and phase angle. Thus DVR is responsible for restoring quality of voltage derived to the end user. The consumer can be isolated from transients and disturbances caused by sags by using DVR. Multilevel inverter based DVR is simulated and the results are presented.

Keywords: *DVR, Multilevel inverter, MATLAB.*

I. INTRODUCTION

Power electronic devices contribute to important part of harmonics in all kind of applications, such as power rectifiers, thyristor converters, and Static VAR Compensators (SVC). The updated Pulse-Width Modulation (PWM) techniques used to control modern static converters such as machine devices, power factor compensators, or active power filters do not produce perfect waveforms, which strongly depend on the semiconductors switching frequency. Voltage or current converters as they generate discrete output waveforms, force the use of machines with special isolation, and in some applications large inductances connected in series with the respective load. In other words, neither the voltage nor the current waveforms are as expected. Also, it is well known that distorted voltages and current waveforms produce harmonic contamination, additional power losses, and high frequency noise that can affect not only the power load but also the associated controllers. All these unwanted operating characteristics associated with PWM converters can be overcome with multilevel converters, in addition to the fact that higher voltage levels can be achieved[1]-[5].

Multilevel inverters can operate not only with PWM techniques but also with Amplitude Modulation (AM), significantly improving the quality of the output voltage waveform. With the use of AM, low frequency voltage harmonics are perfectly eliminated, generating almost perfect sinusoidal waveforms with a Total Harmonic Distortion (THD) lower than 5%. Another important characteristic is that each converter operates at a low switching frequency, reducing the semiconductor stresses, and therefore reducing the switching losses [6], [7]. The principal objective of this paper is to determine the simplest converter topology in terms of the number of power semiconductors for a given number of levels. The "redundant" levels are minimized, and the combination of bridges to maximize the number of levels [8], [9] and minimize power sources and semiconductors are analyzed.

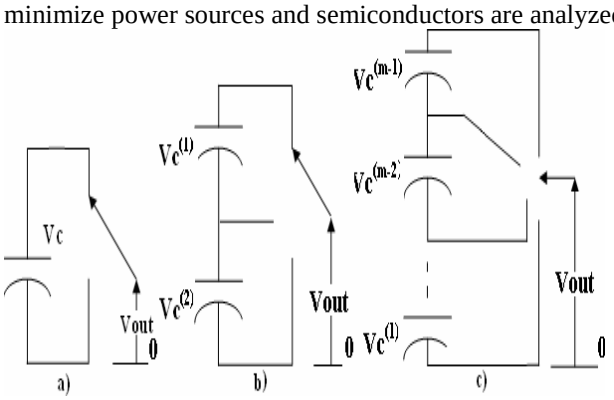


Fig.1. Basic Multilevel inverters (a) two levels, (b) three levels and (c) m levels

II. MULTILEVEL CONVERTER CHARACTERISTICS

The principal function of the inverters is to generate an AC voltage from a DC source voltage. If the DC voltage sources connected in series, it becomes possible to generate an output voltage with several steps. Multilevel inverters include an arrangement of semiconductors and DC voltage sources required to generate a staircase output voltage waveform. Fig. 1 shows the schematic diagram of voltage source-inverters with a different number of levels. It is well known that a two level inverter, such as the one shown in Fig. 1(a), generates an output voltage with two different values (levels) V_c and "zero", with respect to the negative terminal of the dc source ("0"), while a three-level module, Fig, 1(b) generates three different voltages at the output ($2V_c$, V_c and "zero"). The different positions of the ideal switches are implemented with a number of semiconductors that are in direct relation with the output voltage number of levels.

Multilevel inverters are implemented with small DC sources to form a staircase AC waveform, which follows a given reference template. For example, having ten DC

sources with magnitudes equal to 20 V each a composed 11-level waveform can be obtained (five positive, five negatives and zero with respect to the middle point between the ten sources), generating a sinusoidal waveform with 100 V amplitude as shown in Fig. 2, and with very low Total harmonies distortion.

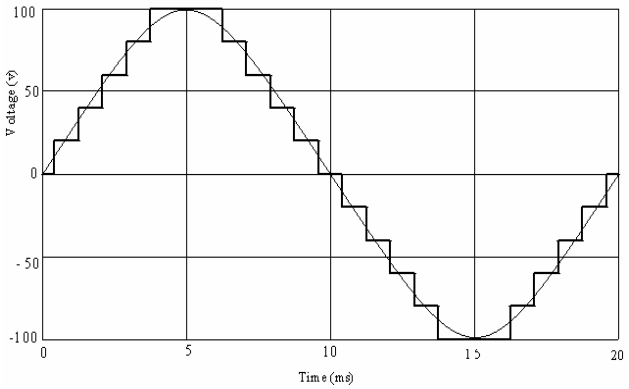


Fig. 2 Voltage waveform from an 11-level inverter

It can be observed that the larger the number of the inverter DC supplies, the greater the number of steps that can be generated, obtaining smaller harmonic distortion. However the number of DC sources is directly related to the number of levels through the equation:

$$n = m - 1 \qquad (1)$$

where n is the number of DC supplies connected in series and m is the number of the output voltage levels. In order to get a 51-level inverter output voltage, 50V supplies would be required, which is too much for a simple topology.

Besides the problem of having to use too many power supplies to get a multilevel inverter, there is a second problem which is also important, the number of power semiconductors required to implement the commutator, as shown in Fig 1. Technical literature has proposed two converter topologies for the implementation of the power commutator, using force-commutated devices [transistors or Gate Turn-Offs (GTOs)]: a) the diode-clamped and b) the capacitor-clamped converter [2].

A. Diode-Clamped Inverter

This inverter consists of a number of semiconductors connected in series, and another identical number of voltage sources, also connected in series. These two chains are connected with diodes at the upper and lower semiconductors as shown in Fig 3 (a). For an m-level converter, the required number of transistors T is given by

$$T = 2\,(m - 1). \qquad (2)$$

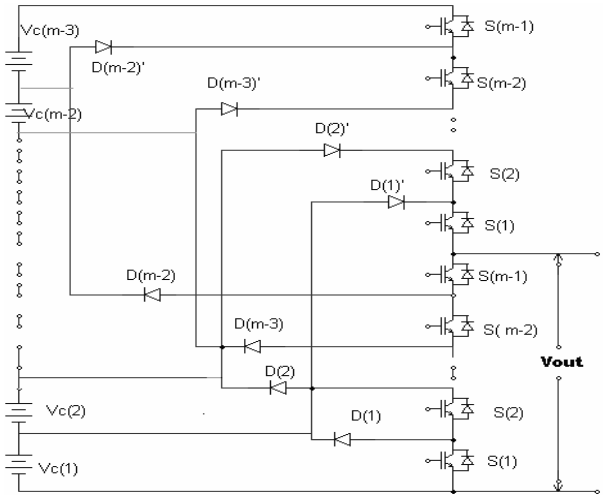
Then, for example of a 51-level converter, 100 power transistors would be required (which is an enormous amount of switches to be controlled). One of the most utilized configurations with this topology is that of the three-level inverter, which is shown in Fig. 3 (b). The capacitors act like two DC sources connected in series. Thus, in the diagram, each capacitor accumulates ½ V_{DC}, giving voltages at the output of ½ V_{DC}, 0, or - ½ V_{DC} with respect to the middle point between the capacitors.

B. Capacitor-Clamped Inverter:

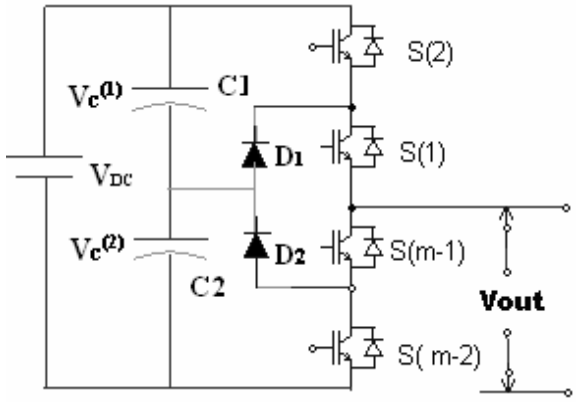
This inverter has a similar structure to that of the diode-clamped, however it can generate the voltage steps with capacitors connected as shown in Fig 4. The problem with this converter is that it requires a large number of capacitors, which translates is that it requires a large number of capacitors, which translates to a bulky and expensive converter as compared with the diode-clamped inverter. Besides, the number of transistors used is the same with the diode-clamped inverter, and therefore, for a 51-level inverter, 100 power transistors are required. In order to overcome all these problems, a third topology, which will be called the "transistor-clamped inverter" will be presented and analyzed.

C. Transistor-Clamped Inverter:

The transistor-clamped inverter has the advantage of requiring the same number of power transistors as the levels generated, and therefore, the semiconductors are



(a)



(b)

Fig. 3 (a) The m-level and (b) three-level diode clamped inverter topology

reduced by half with respect to the previous topologies. A 51-level converter requires 51 transistors (instead of 100

transistors). For an m-level transistor clamped inverter, which satisfies

$$T = m. \quad (3)$$

In this topology, the control of the gates is very simple because only one power transistor is switched-on at a time.

Then, there is a direct relation between the output voltage, V_{out} and the transistor that has to be turned-on. However, and despite the excellent characteristics of this topology, the number of transistors is still too large to allow the implementation of a practical converter with more than 50 levels.

One solution for increasing the number of steps could be the use of "H" converters, like the one shown in Fig 5, which consists of connecting two of the previously discussed Diode and Capacitor clamped topologies in series (two legs). If transistor-clamped inverters are used to build an "H" converter, the number of transistors required for an m-level inverter is m+1, which means only one more transistor than what is required for a simple leg configuration. However, the number of DC source is reduced to 50%, which is the most important advantage of "H" converters.

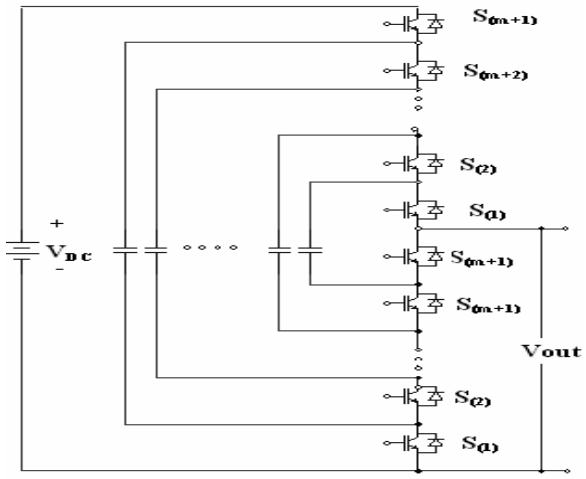


Fig. 4. The m-level capacitor – clamped inverter

Another characteristic is that the "H" topology has many redundant combinations of switch positions to produce the same voltage levels. As an example, the level "zero" can be generated with switches in position S(1) and S(2), or S(3) and S(4), or S(5) and S(6), in fig5(a).

and so on. Another characteristic of "H" converters is that they only produce an odd number of levels, which ensures the existence of the "0-V" level at the load. Shown in fig.5 (b), 5(c)

For example, a 51-level inverter using an "H" configuration with transistor-clamped topology requires 52 transistors, but only 25 power supplies instead of the 50 required when using a single leg. Therefore, the problem related to increasing the number of levels and reducing the size and complexity has been partially solved, since power supplies have been reduced to 50%.

Output Voltage (V)	SWITCHING SEQUENCE							
	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	0	0	0	0	0	0
V1	1	1	0	0	0	0	0	0
V2	0	0	1	1	1	1	0	0
V3	0	0	0	0	1	1	0	0
V4	1	1	0	0	1	1	0	0
V3	0	0	0	0	1	1	0	0
V2	0	0	1	1	1	1	0	0
V1	1	1	0	0	0	0	0	0
-V1	0	0	1	1	0	0	0	0
-V2	1	1	0	0	0	0	1	1
-V3	0	0	0	0	0	0	1	1
-V4	0	0	1	1	0	0	1	1
-V3	0	0	0	0	0	0	1	1
-V2	1	1	0	0	0	0	1	1
-V1	0	0	1	1	0	0	0	0

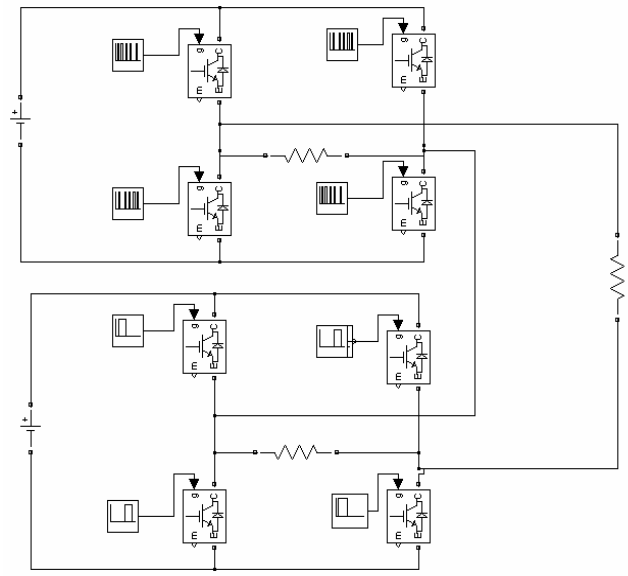


Fig. 5(a) Simulation circuit of cascaded nine-level inverter

III. SIMULATION OF CASCADED NINE-LEVEL INVERTER

By Applying Nine-Level inverter the cascaded nine-level inverter has been simulated using MATLAB software. The simulation circuit is illustrated in Fig. 5(a). The voltage of the cascaded nine- level inverter can be synthesized from the following switching combinations.

The table 1 shows the switching sequence. The driving pulses for switches S1 & S2 are shown in following Fig. 5(b). The driving pulses for switches S5 & S6 are shown in following Fig. 5(c). The Fig. 5(d) shows the output voltage across inverter 1. The Fig. 5(e) shows the output voltage across inverter 2. Nine level inverter output is shown in Fig. 5(f). The frequency spectrum for the output inverter is shown in Fig. 5(g).

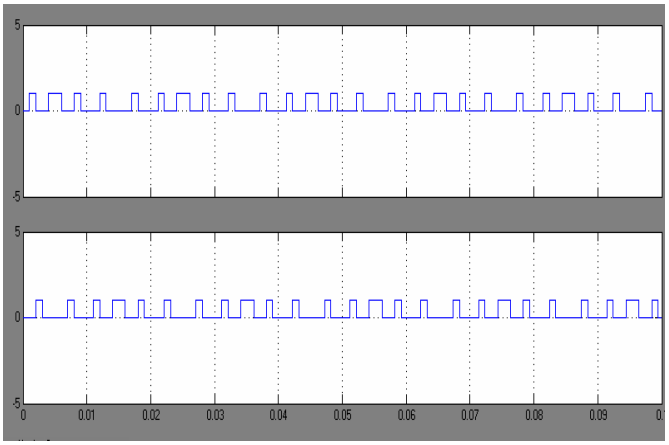


Fig.5(b). Driving pulses for S1 & S_2

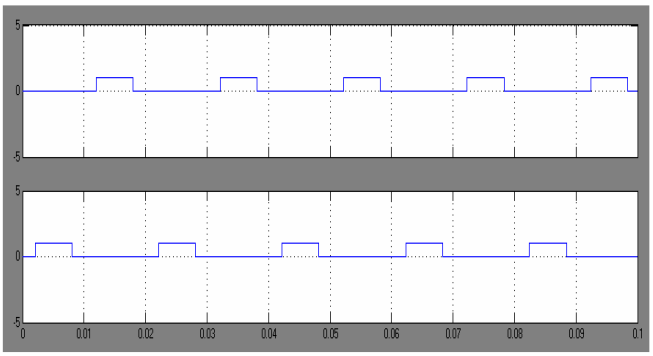


Fig.5(c). Driving pulses for S_5 & S_6

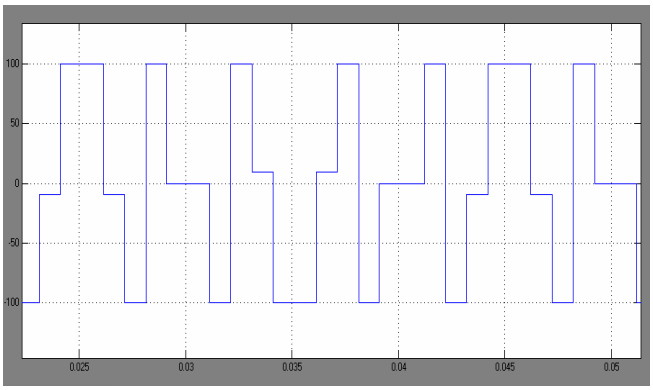


Fig. 5(d). Output voltage across inverter-1

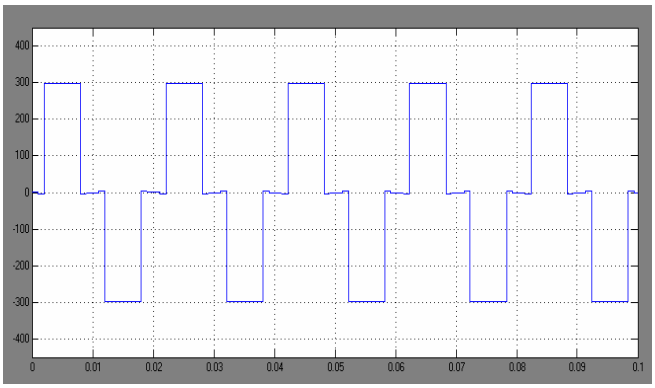


Fig. 5(e). Output voltage across inverter-2

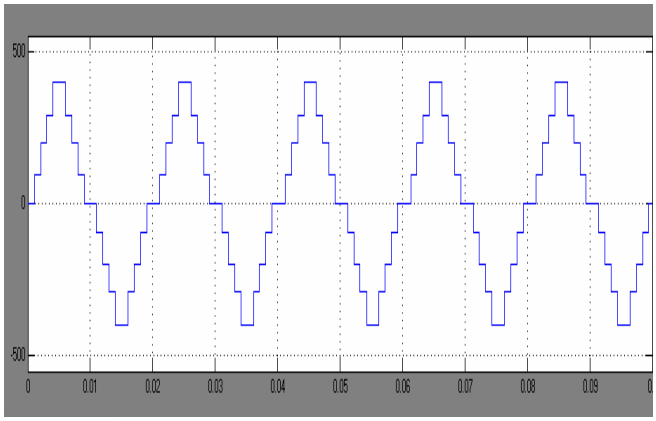


Fig. 5(f). Output of nine-level inverter

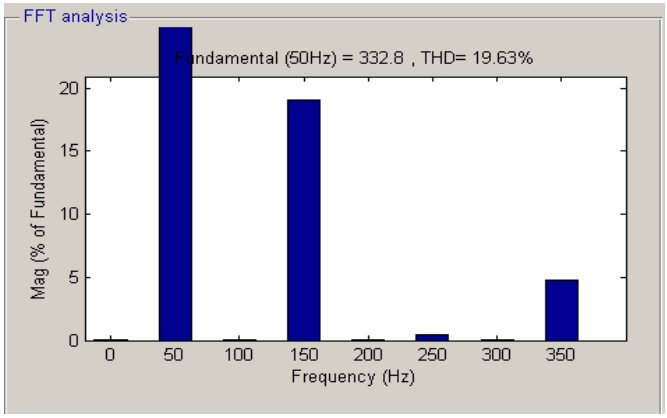


Fig. 5(g). Frequency spectrum for output voltage

IV. CONCLUSION

By using Nine-Level inverter we have analyzed that the dynamic voltage restorer is used to improve voltage sags caused by abrupt increase in loads. Multilevel inverters with large number of steps have been used in the DVR system. Multilevel inverter which requires minimum power supplies have been used in DVR system. The DVR can tackle the problem of harmonics caused by non linear loads in manufacturing industries. In Major Industries can also use DVR to compensate voltage sag. This paper shows simulation results of nine-level inverter based DVR. From the results we obtained that Total Harmonic Distortion is found to be much less than that of single PWM inverter. The simulation results are similar to the analytical predictions

V. REFERENCES

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